Design and Analysis of Low Power Double Tail Comparator for 2-bit Fast ADC

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***Abstract*— Comparator holds a dominant place in fast ADC circuit for the conversion of analog to digital signal. In this modernized digital world every utilization circuits requires an ADC's with low power to consumption. This in turn reflects in the design of comparators during the design process of the fast ADC circuits, scope is due to the higher number of comparator usage. As the technologies are scaling down, the number of transistor per unit area increases, so that the sub threshold leakage current increases which leads to power consumption in any circuit. This sources the project idea to design a comparator. It is presumed during the design that, it consumes low power in its double tail configuration which when replaces an inverter circuit in latch stage of the double tail comparator by a sleepy inverter. This presumption is validated through the analysis of the simulation results. The power consumption of the designed proposed double tail comparator is 30µw when compared to 35 µw in the conventional type. 2-bit flash ADC circuit is designed and analyzed under two different configurations of the double tail comparator. From the results, it is clear that the power consumption of the ADC circuit designed with proposed sleepy inverter based double tail comparator is observed to be 45mw.**

Keywords—sleepy inverter; double tail comparator;analog to digital comparator,leakage current

I. INTRODUCTION

In an open loop configuration, the operational Amplifier finds number of nonlinear applications. e.g. comparators, detectors, limiters and digital interfacing devices namely converter. The comparator is a circuit which compares a signal voltage and the reference voltage. The regenerative comparator consists of the positive feedback and is normally used to provide the high gain and the speed. The dynamic comparator is the regenerative comparator and in which the positive feedback can be obtained by connecting the back to back connected inverter circuit and will act as a latch or the memory element. The Dynamic comparator depends on the clock signal and makes the decision based on whether the applied input signal is higher or lower at the applied clock cycle. It finds more application in the modern world such as analog to digital converter, memory bit line detectors and receivers.

The threshold voltage and gate oxide thickness are scaled down by reducing the channel length of the device. Because of the reduction in threshold voltage the leakage current in the device gets increases exponentially [13]. Theoretically the device will starts conducting when gate source voltage is greater than the threshold voltage (Vgs > Vt). But it will not be applicable for the device at practical condition. When the transistor is in off state the shorter channel length due to the technology scaling causes the sub threshold current to increase. This current causes the power dissipation during the inactive mode of the transistor. This leakage current is the limiting factor in the transistor scaling, as it gets increases when the number of transistor increases per unit area. The leakage current for the MOSFET is given by

$$I_{DS} = I_{DS0} e^{\frac{(V_{GS} - V_T)}{nV_T}} \left[1 - e^{\left(\frac{-V_{DS}}{V_T}\right)} \right]$$

$$V_T = V_{T0} - \eta V_{DS} + \gamma \left[\left(\phi_s + V_{SB} \right)^{0.5} - \left(\phi_s \right)^{0.5} \right]$$

In which the I_{DSO} is current at threshold, V_{TO} is the zero bias threshold voltage, γ is linearised body effect coefficient, η represents the effect of V_{DS} on threshold voltage, n is the sub-threshold swing coefficient, V_T is threshold voltage, V_{SB} source to bulk voltage and V_{GS} is gate source voltage respectively. By increasing the threshold voltage the leakage current decreases. This can be achieved by increasing the source to bulk voltage or by decreasing the gate source voltage, drain source voltage. The literature shows that there are number of comparator available such as Conventional Dynamic Comparator, Conventional Double Tail Dynamic Comparator, and Double Tail Comparator. In which this project focuses on the reduction of power in the double tail comparator.

II. DOUBLE TAIL COMPARATOR

The double tail comparator consists of back to back connected inverter circuit as latch and the preamplifier stage in which the two inputs are given. This circuit operates in two modes one is at reset phase and the other is at decision making phase. The circuit produces the output only at decision making phase and at reset phase the output is at zero values. When clock is zero the circuit works in the reset phase, at which both the tail transistors are OFF and both the fn and fp nodes gets charged by the transistor M9 and M12. These two nodes turn ON the M7 and M8 transistor and this makes both the output nodes outp and outn to zero. When clock is at one condition the circuit operates in the decision making phase. During which both fn and fp nodes discharges depending on the given input signal inp and inn. When input inn is higher, then the node fp discharges faster when compared to fp and this fn node charges the fp node again by turning ON the transistor M11.

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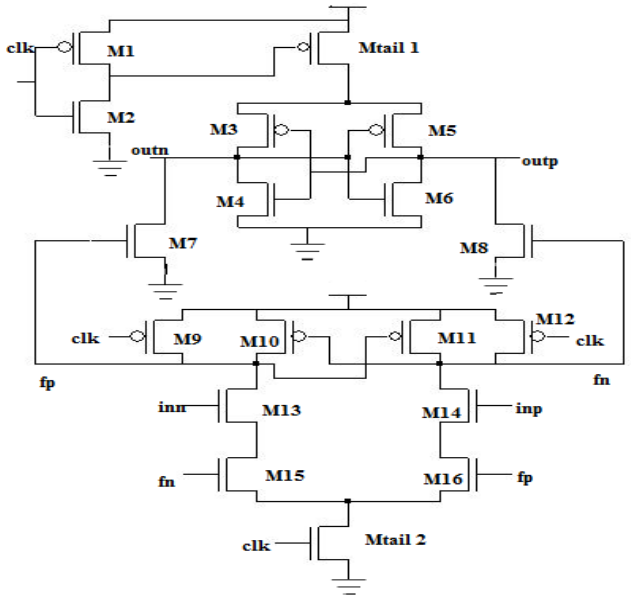

Fig.1 Double Tail Comparator

This makes the outp to zero by switching ON the transistor M8. When this outp is given to the inverter formed by pair of M3 and M4 transistor the outn becomes one. The static power consumption is less in this circuit. The power consumed by this comparator circuit is 35µw .

III. SLEEPY INVERTER

The inverter circuit in the latch stage of the double tail comparator is replaced by the sleepy inverter circuit. In the sleepy inverter circuit the PMOS is placed below the supply and the NMOS is placed above the ground terminal. This sleepy inverter is operating in two modes such as active mode and sleepy mode.

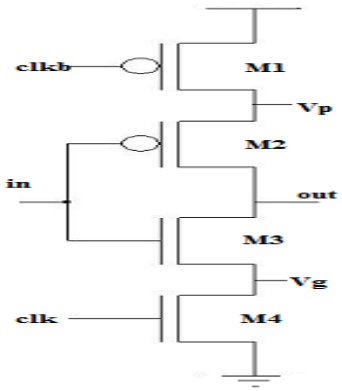

Fig.2 Sleepy Inverter

During the active mode the circuit act as a normal inverter and in sleepy mode there is no current flow in the circuit. When the applied clk is one and clkb is zero, then the circuit operates in the active mode. During which the transistor M1 and M4 conducts and the node Vp is at high potential and the node Vg at ground potential. So the circuit operates as normal inverter. When the applied clk is zero and clkb is one, then the circuit operates in sleepy mode. During which the transistor M1 and M4 turns OFF and the node Vg and Vp is at virtual power potential and virtual ground potential. The potential at Vg increases and the potential at Vp decreases due to the cut off transistors M1 and M4. The source to body potential of transistor M1 increases, so the threshold voltage increases and hence the leakage current and the power consumption get decreases. The main drawback of the sleepy inverter concept is that, it losses the state information during the sleep mode of operation.

IV. PROPOSED DOUBLE TAIL COMPARATOR

The proposed double Tail Comparator is shown in be fig. 3. In which the inverter in the latch circuits is replaced by the sleepy inverter. The operation of the proposed double tail comparator remains same as the double tail comparator.

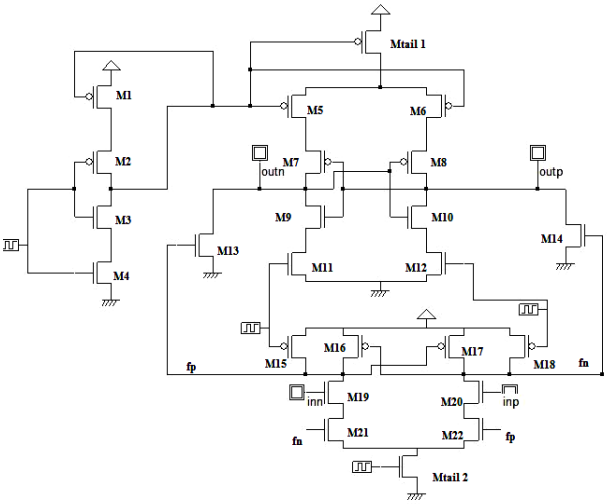

Fig. 3 Proposed Double Tail Comparator(with Sleepy inverter)

During normal mode the drain of M5 and M6 is at high potential and drain of M11 and M12 at ground potential. At sleep mode all the M5,M6,M11 and M12 are cut off. By incorporating the sleepy inverter in the proposed double tail comparator the overall power consumption of the circuit is reduced.

V. BLOCK DIAGRAM OF FLASH ADC CIRCUIT

Flash analog to digital converters, also known as parallel ADCs, are the fastest circuit for the conversion of the analog to a digital signal. The Flash type ADC has the least conversion time and is used in time critical applications such as a sample and hold circuit of a digital oscilloscope. The flash type ADC consists of an array of parallel comparators, the potential divider and the priority encoder. In which the analog signal is applied to the non inverting terminal of the comparator and reference voltage is given to the inverting input terminal of the comparator through the potential divider network.

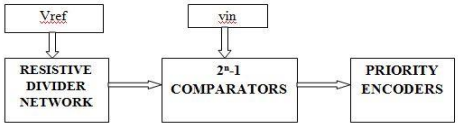

Fig. 4 Block Diagram of Flash ADC circuit

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If the n bit digital output is required then (2^n-1) comparators are used. The priority encoder accepts a 2^n line input and gives out an n bit binary output. Each of the input line has a progressively increasing priority

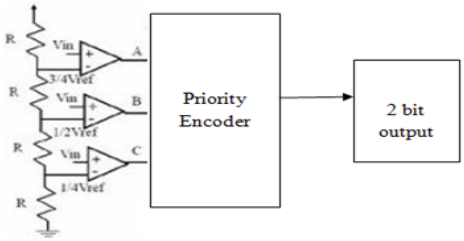

Fig. 5 Block Diagram of Two bit Flash ADC circuit

The two bit flash ADC circuit requires three comparators and priority encoders. This ADC circuit is designed with the designed double tail comparator. When the analog input is between 0 and 1/4 of V_{ref} all comparator produce zero output. When the analog input is between 1/4 and 1/2 of Vref the comparator c only produces 1. When it is between 1/2 and 3/4 of V_{ref} the comparator C and B only produces 1. However, as comparator for C goes high, all comparator below C go high as well. So, a priority encoder is used to convert these input lines form the comparator into binary coded output. The priority encoder includes the priority function. The operation of the priority encoder is such that if two or more inputs are equal to 1 at the same time, the input having the highest priority will take the precedence.

VI. RESULT AND COMPARISON

Both the double tail comparators are simulated with Tanner tool of V14.1. The two comparator circuit is applied with different dc input voltage of inn and inp. In the flash ADC circuit the comparator is fed with the analog signal of amplitude of 30v and the reference voltage of 10v.

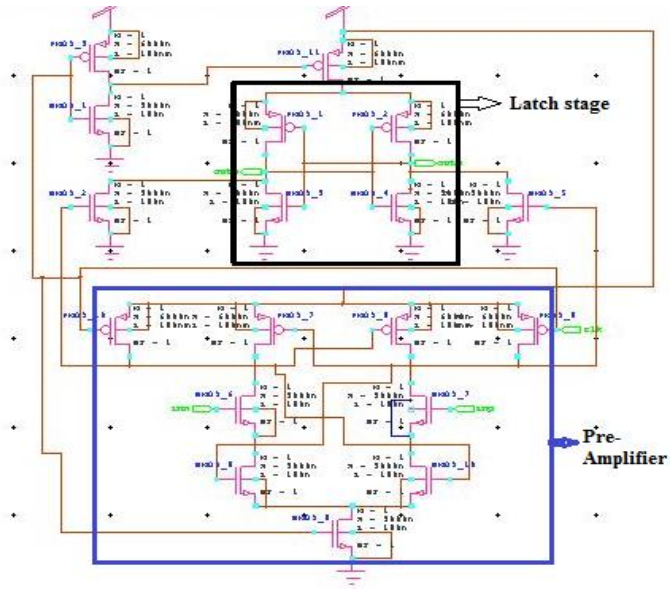

Fig.6 Simulated Double tail comparator

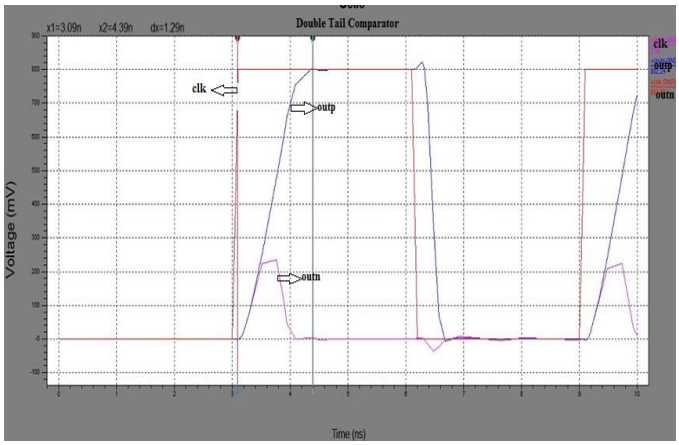

Fig. 7 Output Waveform of Double Tail Comparator

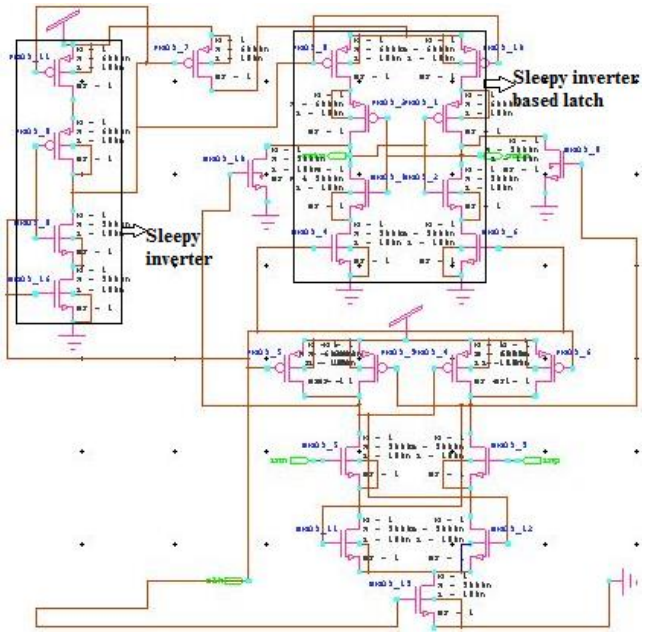

Fig. 8 Simulated Proposed Double Tail comparator

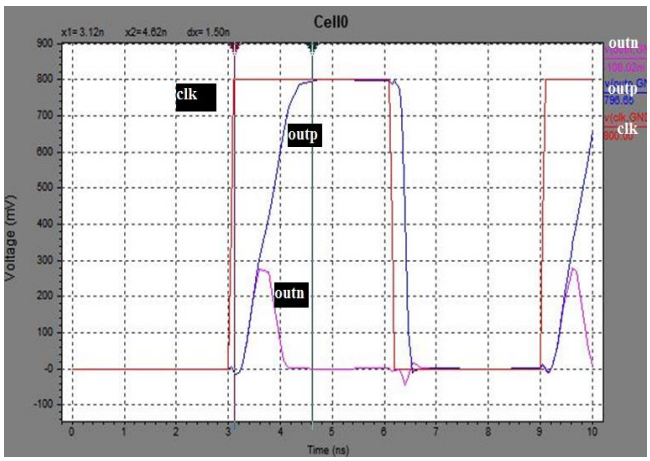

Fig.9 Output waveform of Proposed double tail comparator

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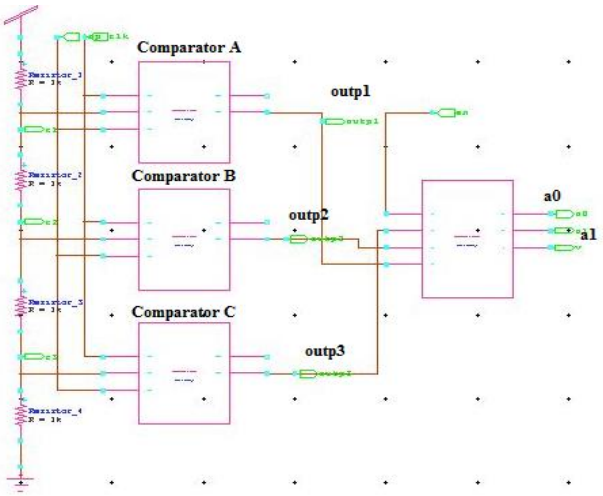

Fig.10 Designed Two bit Flash ADC Circuit

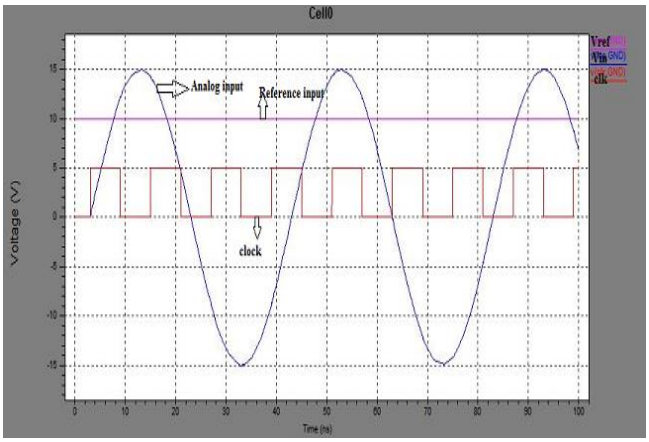

Fig.11 Input Waveform of two bit Flash ADC circuit

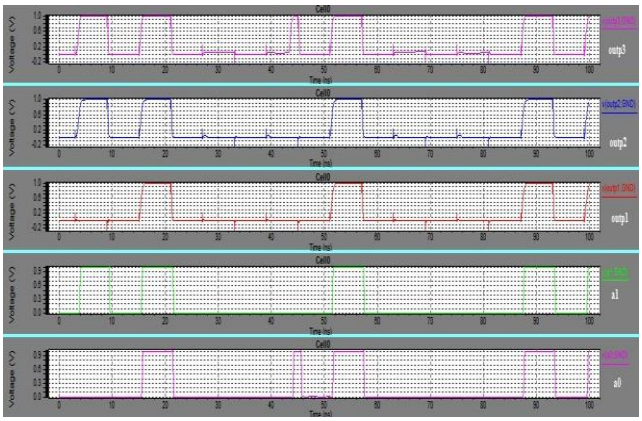

Fig.12 Output and intermediate node Waveform of the Two Bit Flash ADC circuit

The comparison chart shows the power consumed and the delay obtained by the double tail and the proposed double tail comparator. And the power consumed by the different ADC circuit.

Table I

Comparison of Two Designed Comparator

PARAMETERS	MDTDC	PDTC
Technology(nm)	180	180
Power(µw)	35	30
Delay(ns)	1.29	1.50
Transistor Count	18	24
Supply Voltage(v)	0.8	0.8

Table II

Comparison of Two Bit Flash ADC with Different Comparators

Circuit	Power consumption	No of transistor
ADC with Modified Double Tail Dynamic Comparator	4.6*10^-4	92
ADC with proposed Comparator	4.5*10^-4	110

VII. CONCLUSION

All the comparator and the two bit Flash ADC circuit are designed in 180nm CMOS technology using the tanner tool. The proposed double tail comparator designed using the sleepy inverter circuit has the power of 30µw and the two bit flash ADC circuit that is designed with this comparator consumes the power of 45mw which is less when compared to the ADC circuit designed with double tail comparator. So the proposed double tail comparator is best suitable for the two bit flash ADC circuit.

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